What is claimed is:

1. A charge coupled device (CCD) imaging apparatus comprising:

a CCD operable for a progressive scanning;

a drive pulse switching circuit for generating a CCD drive pulse for said CCD at a first frame rate;

a CCD driver for driving the CCD by converting the CCD drive pulse into a specified voltage;

a frame memory for storing an output signal of said CCD; and

a camera signal processing circuit for receiving an output signal of said frame memory and performing a specified camera process,

wherein said drive pulse switching circuit generates a CCD read pulse of the CCD drive pulse at the first frame rate, and generates the CCD drive pulse other than the CCD read pulse at a frame rate (n/2) times as high as the first frame rate, the n being an arbitrary integer, and

wherein said frame memory stores an output signal of said CCD in one frame right after the CCD read pulse, and repeats to read out the stored output signal of said CCD in one frame (n/2) times.

2. The CCD imaging apparatus of claim 1, further comprising a recorder unit for recording a signal output from said camera signal processing circuit at the first frame rate.

3. The CCD imaging apparatus of claim 2, further comprising a first reproduced signal converter for outputting a reproduced signal of said recorder unit selectively at the frame rate (n/2) times as high as the first frame rate and at the first frame rate.

4. The CCD imaging apparatus of claim 3, further comprising:

a viewfinder for displaying a output signal of said camera signal processing circuit; and

a second reproduced signal converter for converting the reproduced signal from said recorder unit to the frame rate (n/2) times as high as the first frame rate, and for outputting the converted signal to said viewfinder.

5. The CCD imaging apparatus of claim 1,

wherein, when the first frame rate is lower than a specified frame rate, said drive pulse switching circuit generates the CCD read pulse for said CCD at the first frame rate, and generates the CCD drive pulse other than the CCD read pulse at the frame rate (n/2) times as high as the first frame rate, and

wherein, when the first frame rate is lower than the specified frame rate, said frame memory stores the output signal of said CCD in one frame right after the CCD read pulse, and repeats to read out the stored output signal of said CCD in one frame (n/2) times.

6. The CCD imaging apparatus of claim 5, wherein the specified frame rate is 30 frames/sec.

7. The CCD imaging apparatus of claim 6, wherein the first frame rate can be set at 24 frames/sec, 25 frames/sec, and 30 frames/sec, and the n is 2.

8. The CCD imaging apparatus of claim 1, wherein said drive pulse switching circuit includes a frame rate equalizing controller for

making said CCD output a signal of the first frame rate and a signal of a second frame rate at a common frame rate of a common multiple of the first and second frame rates, and wherein said pulse switching circuit generates the other CCD drive pulse than the CCD read pulse for said CCD at the common frame rate.

9. The CCD imaging apparatus of claim 8, wherein the common frame rate can be set to 60 frames/sec and 48 frames/sec.

10. The CCD imaging apparatus of claim 9, further comprising a recorder unit for recording a signal from said camera signal processing circuit at the first and second frame rates.

11. The CCD imaging apparatus of claim 10, wherein said recorder unit reproduces a signal at the common frame rate.

12. The CCD imaging apparatus of claim 10, further comprising a first reproduced signal converting circuit for issuing a reproduced signal of said recorder unit selectively at the frame rate (n/2) times as high as the first frame rate and at the first frame rate.

13. The CCD imaging apparatus of claim 12, further comprising:

a viewfinder for displaying an output signal of said camera signal processing circuit; and

a second reproduced signal converter for converting a reproduced signal of said recorder unit to the frame rate (n/2) times as high as the first frame rate, and for issuing the converted reproduced signal to said

viewfinder.

14. The CCD imaging apparatus of claim 1,

wherein said CCD is of a multiple frame interline transfer (MFIT) type for reading out a progressive scanning signal divided into an odd line field and an even line field,

wherein said frame memory outputs the signal in one frame in a segment frame (SF) format by dividing the signal into an odd line field and an even line field,

wherein said drive pulse switching circuit comprises a read field controller for generating a CCD drive pulse to control an order of signals in the odd and even fields output from said CCD,

wherein said read field controller changes the order of the signals in the odd and even fields from said CCD when the n is an odd number at every frame, and

wherein said read field controller does not change the order of the signals in the odd and even fields from said CCD when the n is an even number.

15. A charge coupled device (CCD) imaging apparatus comprising:

a CCD operable for a progressive scanning;

a drive pulse switching circuit for generating a CCD drive pulse for said CCD at a first frame rate;

a CCD driver for driving said CCD by converting the CCD drive pulse into a specified voltage;

a camera signal processing circuit for receiving an output signal of said CCD and performing a specified camera process;

a first frame memory for storing a first signal issued from said camera signal processing circuit, and reading out the stored first signal at a frame rate of the first signal; and

a second frame memory for storing the first signal and reading out the stored first signal at the first frame rate,

wherein said drive pulse switching circuit generates a CCD read pulse of the CCD drive pulse at the first frame rate, and generates the CCD drive pulse other than the CCD read pulse at a frame rate (n/2) times as high as the first frame rate, the n being an arbitrary integer,

said first frame memory stores a signal in one frame of the first signal issued from said camera signal processing circuit right after the CCD read pulse, and repeats to read out the stored first signal (n/2) times, and

said second frame memory stores the first signals, and read out the stored first signal during a period of (n/2) frames.

16. The CCD imaging apparatus of claim 15, wherein said second frame memory increases a number of samples in a horizontal blanking period of the first signal, and reads out the first signal during the period of (n/2) frames.

17. The CCD imaging apparatus of claim 15, further comprising a recorder unit for recording and reproducing a signal issued from said second frame memory at a rate of the signal.

18. The CCD imaging apparatus of claim 15, further comprising a viewfinder for displaying an output signal of said first frame memory.

19. The CCD imaging apparatus of claim 15,

wherein, when the first frame rate is lower than a specified frame rate, said drive pulse switching circuit generates the CCD read pulse for said CCD at the first frame rate, and generates the CCD drive pulse other than the CCD read pulse at the frame rate (n/2) times as high as the first frame rate,

wherein, when the first frame rate is lower than the specified frame rate, said first frame memory stores the first signal, and repeats to read out the stored first signal (n/2) times, and

wherein, when the first frame rate is lower than the specified frame rate, said second frame memory stores the first signal, and reads out the stored first signal during a period of (n/2) frames.

20. The CCD imaging apparatus of claim 19, wherein the specified frame rate is 30 frames/sec.

21. The CCD imaging apparatus of claim 20, wherein the first frame rate can be set at 24 frames/sec, 25 frames/sec, and 30 frames/sec, and the n is 4.

22. The CCD imaging apparatus of claim 14, further comprising a first reproduced signal converter for issuing a reproduced signal of said recorder unit selectively at the frame rate (n/2) times as high as the first frame rate and at the first frame rate.

23. The CCD imaging apparatus of claim 22, further comprising a

second reproduced signal converter for converting a reproduced signal of said recorder unit to a signal of the frame rate (n/2) times as high as the first frame rate, and

a switching circuit for selectively issuing outputs of said first frame memory and said second reproduced signal converter.

24. The CCD imaging apparatus of claim 14, further comprising a power on/off circuit for turning off said camera signal processing circuit except a period when said camera signal processing circuit outputs the first signal.